IN THE CLAIMS:

1-53. (Canceled)

54. (Previously Presented) A method for forming a structure for an integrated circuit comprising:

(a) depositing a layer of a refractory metal upon a substrate;

(b) forming a layer of metal nitride on said refractory metal, wherein said metal nitride layer is formed using a gas comprising a metallo-organic substance; and

(c) exposing the metal nitride layer to a plasma to reduce the resistivity of said layer by removing carbon from the metal nitride layer.

55. (Currently Amended) The method of claim 54, wherein said metal nitride layer has thickness of less than 130 Å.

56. (Previously Presented) The method of claim 54, wherein said metal nitride layer has a thickness in the range of 25 to 75 Å.

57. (Previously Presented) The method of claim 54, wherein said layer of said refractory metal and said metal nitride layer have a combined thickness of less than 200 Å.

58. (Previously Presented) The method of claim 54, wherein said plasma comprises at least one gas selected from the group consisting of nitrogen, hydrogen, argon, helium, and ammonia.

59. (Previously Presented) The method of claim 54, wherein said metal nitride layer comprises titanium.

60. (Previously Presented) The method of claim 54, wherein said plasma comprises a noble gas.

61. (Previously Presented) The method of claim 54, wherein said step of depositing said metal nitride and said step of exposing the metal nitride to a plasma are both performed in a single chamber.

62. (Previously Presented) The method of claim 54 further comprising biasing the substrate while exposing the metal nitride layer to the plasma.

63. (Currently Amended) The method of claim ~~54~~ 62, wherein the biasing step produces a DC self-bias on the substrate.

64. (Previously Presented) The method of claim 54 wherein said metallo-organic substance is tetrakis (dialkylamido) titanium.

65. (Previously Presented) The method of claim 54, wherein said step of exposing the metal nitride layer to the plasma comprises:

exposing said metal nitride layer to a first plasma; and

exposing said metal nitride layer to a second plasma after exposing said metal nitride layer to said first plasma.

66. (Previously Presented) The method of claim 65 further comprising biasing the substrate while exposing the metal nitride layer to the first plasma and the second plasma.

67. (Previously Presented) The method of claim 65, wherein said first plasma comprises at least one gas selected from the group consisting of nitrogen, hydrogen, argon, helium, and ammonia.

68. (Previously Presented) The method of claim 65, wherein said second plasma comprises at least one gas selected from the group consisting of nitrogen, helium, neon, and argon.

69. (Currently Amended) The method of claim 54, wherein said refractory metal is a metal selected from the group consisting of titanium, ~~tungsten,~~ tantalum, cobalt, and molybdenum.

70. (Currently Amended) A method for forming a barrier layer for an integrated circuit comprising:

(a) depositing a first layer of titanium ~~or tungsten~~ upon a substrate;

(b) depositing a second layer of titanium nitride on said first layer wherein said second layer is formed using a gas comprising a metallo-organic substance and said second layer has a thickness of less than 130 angstroms; and

(c) exposing the second layer to a plasma comprising at least one of nitrogen or hydrogen to reduce the resistivity of said second layer by removing carbon from the second layer.

71. (Previously Presented) The method of claim 70 wherein the metallo-organic substance is tetrakis (dialkylamido) titanium.

72. (Currently Amended) The method of claim 70, further comprising:

biasing the substrate while exposing the ~~metal nitride~~ second layer to a plasma.

73. (Previously Presented) The method of claim 72 wherein a bias established by the biasing step is a DC self bias.

74. (Previously Presented) The method of claim 70 wherein the first layer depositing step is performed using physical vapor deposition.

75. (Currently Amended) A method of forming on a substrate an interconnect structure for an integrated circuit having gate ~~widths~~ lengths that are less than or equal to 0.25 mm comprising:

depositing a titanium layer in contact with a conductive silicon containing material using physical vapor deposition to a thickness of 100Å or less;

depositing a titanium nitride layer upon the titanium layer using chemical vapor deposition of a metal-organic substance to a thickness of 100Å or less;

plasma annealing the titanium nitride layer to improve the resistivity of the titanium nitride layer by removing carbon from the titanium nitride layer; and

depositing a metal layer in contact with the titanium nitride layer.

76. (Previously Presented) The method of claim 75 wherein the titanium layer depositing step further comprises:

using a collimator to guide titanium from a target to a substrate.

77. (Previously Presented) The method of claim 75 wherein the titanium layer depositing step further comprises:

using an ionization coil to guide titanium from a target to the substrate.

78. (Previously Presented) The method of claim 75 wherein the plasma annealing step further comprises:

biasing the substrate while performing plasma annealing.

79. (Cancelled)

80. (Currently Amended) The method of claim ~~79~~ 75, wherein the metallo-organic substance is tetrakis (dialkylamido) titanium.